REMARKS

Claims 9-18 are pending in the application upon entry of the amendments and new claims. Claims 9, 11, and 12 have been amended for clarification purposes. Claims 1-8 have been cancelled. Claims 15-18 have been added. Favorable reconsideration in light of the amendments and the remarks which follow is respectfully requested.

The Amendments

The claims have been amended to clarify the type of devices for the ESD protection is provided, and specifically, to disclaim DRAM devices in order to avoid any unnecessary confusion with Wu (cited below). New claims have been added to further describe the invention. For example, new claims 16-18 describe implantation parameters. New claims 15, 17, and 18 specify that the core region is masked when heavily doping source and drain regions for the electrostatic discharge protection transistors.

The Indefiniteness Rejection

Claim 11 has been rejected under 35 U.S.C. § 112, second paragraph, with regard to the limits of the claim. Claim 11 has been amended to clearly define its subject matter by describing implantation parameters.

The Obviousness Rejection

Claims 9, 10, 12, and 13 have been rejected under 35 U.S.C. § 103 over Wu (U.S. Patent 6,008,081) in view of Reisinger (U.S. Patent 6,137,718). Claim 14 has been rejected under 35 U.S.C. § 103 over Wu in view of Reisinger further in view of Wilson et al.

Wu relates to making an ESD protection structure in an DRAM device. Referring to Figure 2, Wu involves forming a large ESD structure of an insulating layer and

polysilicon; performing an LDD implant; forming a temporary spacer about the ESD structure; performing an HDD implant; dividing the ESD structure in half, removing the temporary spacer; performing a third implant; and forming a spacer about the divided ESD structures. Reisinger is cited for the proposition of describing SONOS devices.

There are several differences between the claims and Wu. Initially, it is noted that Wu relates to DRAM devices while the claims are directed to non-volatile memory devices. This is important because ESD can have different effects on DRAM devices versus non-volatile memory devices. For example, undesirable short channel effects are frequently encountered in non-volatile memory devices. As a result, DRAM devices and non-volatile memory devices require different forms of ESD protection, and thus the manner of ESD protection in one type of device does not necessarily suggest an appropriate type of protection in the other type of device.

Another difference between the claims and Wu is the structure of the ESD transistors of the claims versus the ESD circuit structures of Wu. The ESD structures of Wu are made of two gates (90 and 91 in Figure 2D) connected by a polysilicon layer (96b in Figure 2F). The two gates have two source/drains (80b and 80c in Figure 2F) source/drain 80b is formed by the first, second and third implant while source/drain 80c is formed by only the third implant. Spacers (92 in Figure 2F) on the two ESD gates (90 and 91 in Figure 2D) are formed AFTER the first, second, and third implantations are performed. Therefore, the source/drains of Wu are adjacent the gates. In contrast the heavily doped source/drains of the ESD transistors of the claims are not adjacent the transistors, but instead spaced a safe distance away from ESD transistors. Consequently, the ESD transistors of the claims avoid the short channel effects induced by heavy implants that are adjacent the gates.

Yet another difference between the claims and Wu is the manner or methodology in which ESD protection is fabricated. Wu fails to teach or suggest performing a heavy ESD implant after forming the spacers. As mentioned in the paragraph above, spacers (92 in Figure 2F) on the two ESD gates (90 and 91 in Figure 2D) are formed AFTER the

first, second, and third implantations are performed. This results in structural and functional differences in the devices. The structural differences are highlighted in the paragraph above. The functional differences illustrate the advantages of the claimed invention.

One of the problems associated with heavily doped source/drains adjacent ESD structures is the occurrence of short channel effects. Applying the teachings of Wu to non-volatile memory devices would thus result in undesirable short channel effects. The claimed invention overcomes this problem by performing a heavy implant on the ESD transistors after forming spacers so that: 1) the ESD transistor retains a relatively small length, and 2) the heavy implant is not adjacent the ESD transistor. Wu fails to teach or suggest both of these aspect of the claimed invention. Due to the fatal flaws of Wu, one skilled in the art would not have been motivated by Wu to practice the claimed method.

Although Reisinger mentions SONOS devices, Reisinger fails to cure the deficiencies of Wu. In particular, Reisinger fails to teach or suggest performing a heavy ESD implant after forming spacers for an ESD transistor. Therefore, for this additional reason, the claims are unobvious and therefore patentable.

Should the Examiner believe that a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact Applicants' undersigned attorney at the telephone number listed below.

In the event any fees are due in connection with the filing of this document, the Commissioner is authorized to charge those fees to our Deposit Account No. 50-1063.

Respectfully submitted,

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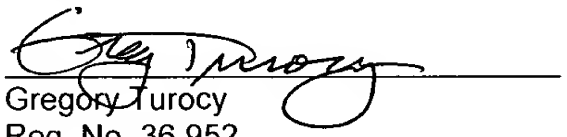

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VERSION OF AMENDMENTS WITH MARKINGS TO SHOW CHANGES

In the Claims:

Please amend the claims in the below-indicated manner.

9. (Amended) A method of forming [an integrated circuit] non-volatile semiconductor memory device, comprising:

providing a semiconductor substrate having a core region and a peripheral region;

forming one or more insulating layers for one or more electrostatic discharge protection transistors and one or more other transistors in the peripheral region;

forming a poly layer over the insulating layers;

patterning electrostatic discharge protection transistors and other transistors from the insulating layers and the poly layer;

depositing spacer material over the electrostatic discharge protection transistors and the other transistors;

etching the spacer material to form spacers; and

with the spacers in place, heavily doping source and drain regions for the electrostatic discharge protection transistors.

11. (Amended) The method of claim 10, wherein [the heavy doping would cause a short channel effect in the electrostatic discharge protection transistors were it not for the spacers] heavily doping source and drain regions involves implanting with one of arsenic and phosphorus at about 5 x 10^{14} atoms/cm^2 to about 7 x 10^{15} atoms/cm^2 at an energy from about 60 keV to about 100 keV.

12. (Amended) The method of claim 9, wherein the [integrated circuit] non-volatile semiconductor memory device is a SONOS type flash memory device.

Please cancel claims 1-8 without prejudice.

Please add the following new claims.

15. (Added) The method of claim 9, wherein the core region is masked when heavily doping source and drain regions for the electrostatic discharge protection transistors.

16. (Added) The method of claim 9, wherein heavily doping source and drain regions involves implanting with one of arsenic and phosphorus at about 1×10^{14} atoms/cm^2 to about 1×10^{16} atoms/cm^2 at an energy from about 60 keV to about 100 keV.

17. (Added) A method of forming non-volatile semiconductor memory device, comprising:

providing a semiconductor substrate having a core region and a peripheral region;

forming one or more insulating layers for one or more electrostatic discharge protection transistors and one or more other transistors in the peripheral region;

forming a poly layer over the insulating layers;

patterning electrostatic discharge protection transistors and other transistors from the insulating layers and the poly layer;

lightly doping source and drain regions for the electrostatic discharge protection transistors with one of arsenic, boron, and phosphorus at about 1×10^{11} atoms/cm^2 to about 1×10^{14} atoms/cm^2 at an energy from about 20 keV to about 80 keV;

depositing spacer material over the electrostatic discharge protection transistors and the other transistors;

etching the spacer material to form spacers; and

with the spacers in place, heavily doping source and drain regions for the electrostatic discharge protection transistors with one of arsenic and phosphorus at about 1 x 10^{14} atoms/cm^2 to about 1 x 10^{16} atoms/cm^2 at an energy from about 60 keV to about 100 keV.

18. (Added) A method of forming non-volatile semiconductor memory device, comprising:

providing a semiconductor substrate having a core region and a peripheral region;

forming one or more insulating layers for one or more electrostatic discharge protection transistors and one or more other transistors in the peripheral region;

forming a poly layer over the insulating layers;

patterning electrostatic discharge protection transistors and other transistors from the insulating layers and the poly layer;

lightly doping source and drain regions for the electrostatic discharge protection transistors with one of arsenic, boron, and phosphorus at about 1 x 10^{11} atoms/cm^2 to about 1 x 10^{14} atoms/cm^2 at an energy from about 20 keV to about 80 keV;

depositing spacer material over the electrostatic discharge protection transistors and the other transistors;

etching the spacer material to form spacers; and

with the spacers in place, masking the core region and heavily doping source and drain regions for the electrostatic discharge protection transistors with one of arsenic and phosphorus at about 5 x 10^{14} atoms/cm^2 to about 7 x 10^{15} atoms/cm^2 at an energy from about 60 keV to about 100 keV.